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Dhandapani et al.

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(54) **ROBUST PILLAR STRUCTURE FOR SEMICONDCUTOR DEVICE CONTACTS**

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H01L 23/498 (2006.01)
H01L 23/00 (2006.01)
H01L 21/48 (2006.01)

(52) **U.S. Cl.**
CPC ***H01L 23/49811*** (2013.01); ***H01L 24/11*** (2013.01); *H01L 21/4853* (2013.01); *H01L 24/12* (2013.01); *H01L 24/13* (2013.01); *H01L 24/14* (2013.01); *H01L 24/15* (2013.01)

(58) **Field of Classification Search**
CPC H01L 24/16
See application file for complete search history.

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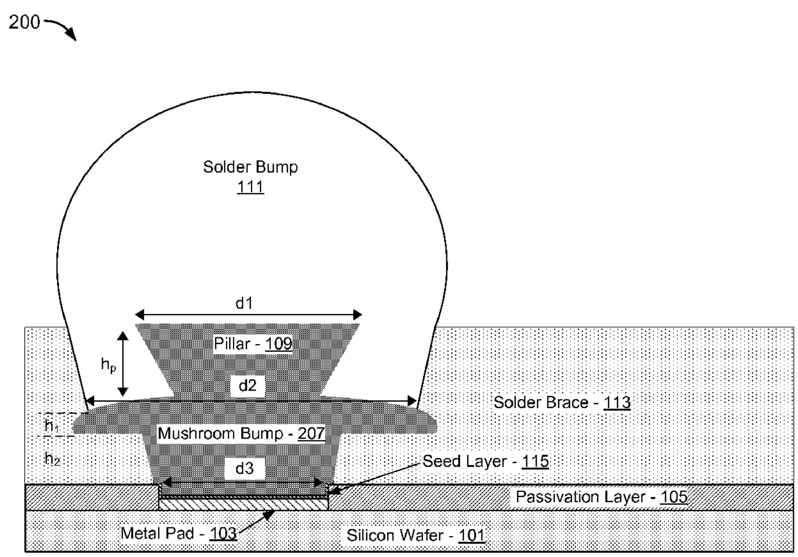
(57) **ABSTRACT**

Methods and systems for a robust pillar structure for a semiconductor device contacts are disclosed, and may include processing a semiconductor wafer comprising one or more metal pads, wherein the processing may comprise: forming a second metal contact on the one or more metal pads; forming a pillar on the second metal contact, and forming a solder bump on the second metal contact and the pillar, wherein the pillar extends into the solder bump. The second metal contact may comprise a stepped mushroom shaped bump, a sloped mushroom shaped bump, a cylindrical post, and/or a redistribution layer. The semiconductor wafer may comprise silicon. A solder brace layer may be formed around the second metal contact. The second metal contact may be tapered down to a smaller area at the one or more metal pads on the semiconductor wafer. A seed layer may be formed between the second metal contact and the one or more metal pads on the semiconductor wafer. The pillar may comprise copper.

22 Claims, 14 Drawing Sheets



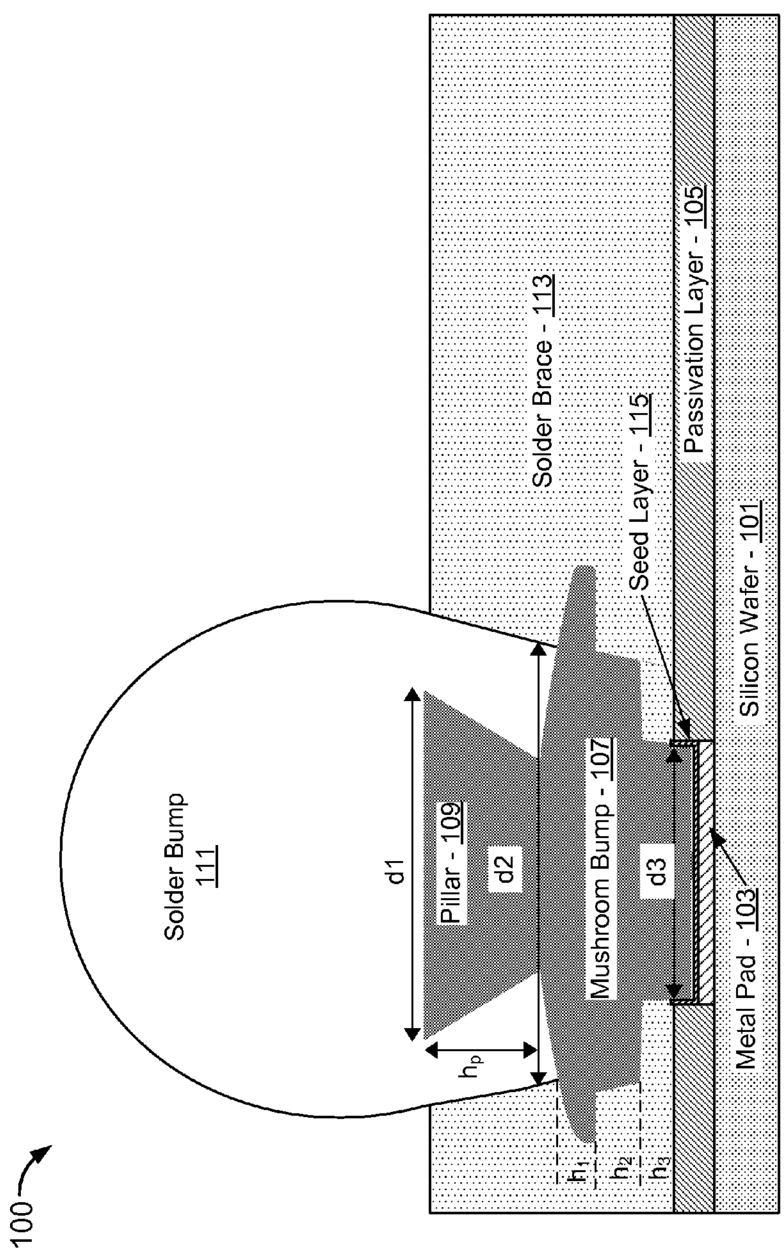

100
Solder Bump
111
Pillar - 109
d1
d2
h_p
Mushroom Bump - 107
d3
Solder Brace - 113
Seed Layer - 115
Passivation Layer - 105
Silicon Wafer - 101
Metal Pad - 103
h_1
h_2
h_3

FIG. 1

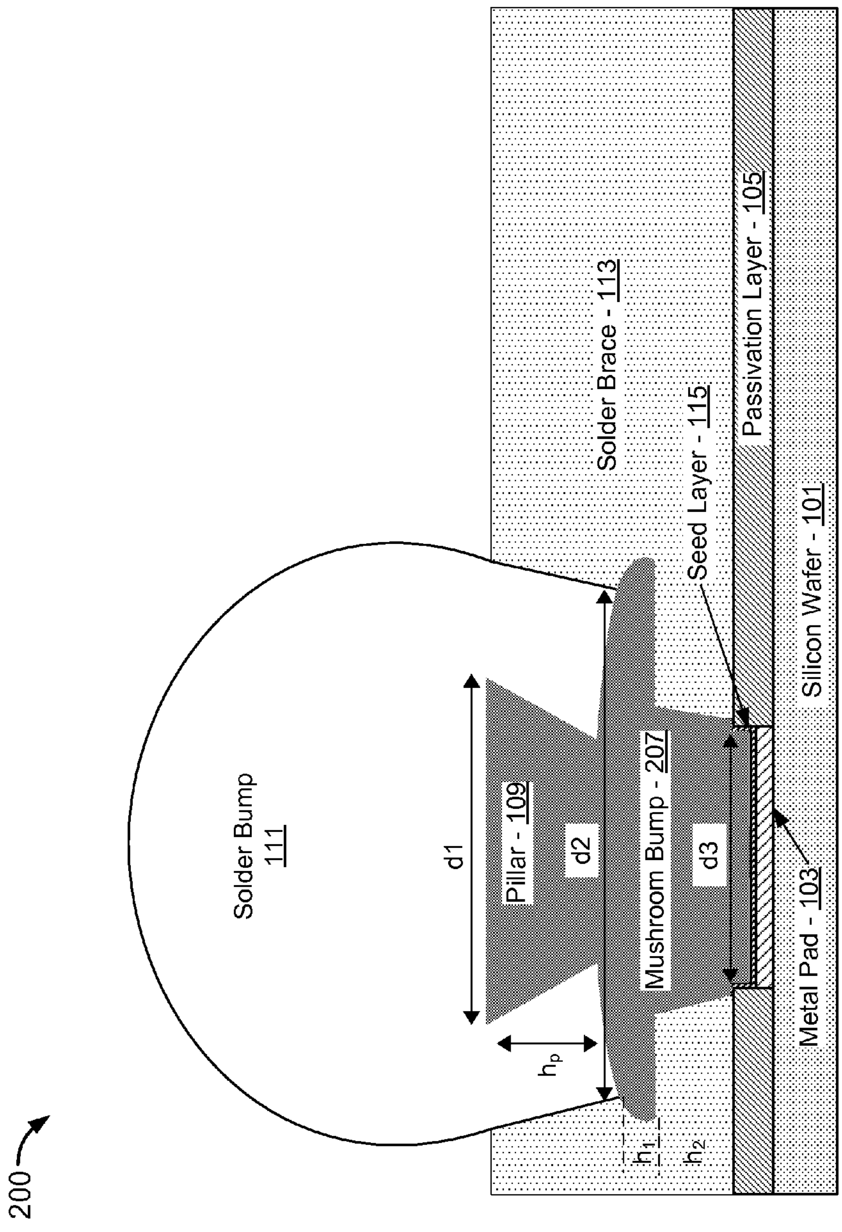

200
Solder Bump 111
Pillar - 109
Mushroom Bump - 207
Solder Brace - 113
Seed Layer - 115
Passivation Layer - 105
Silicon Wafer - 101
Metal Pad - 103
d1
d2
d3
h_p
h_1
h_2

FIG. 2

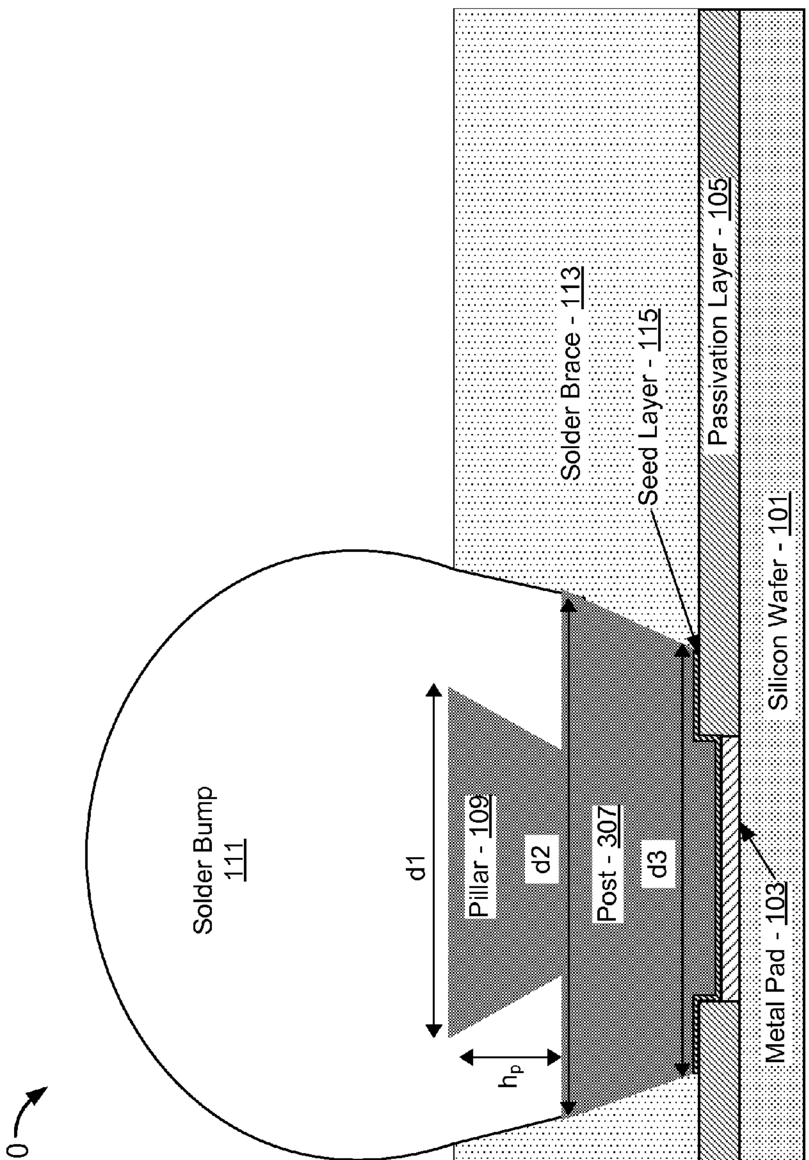
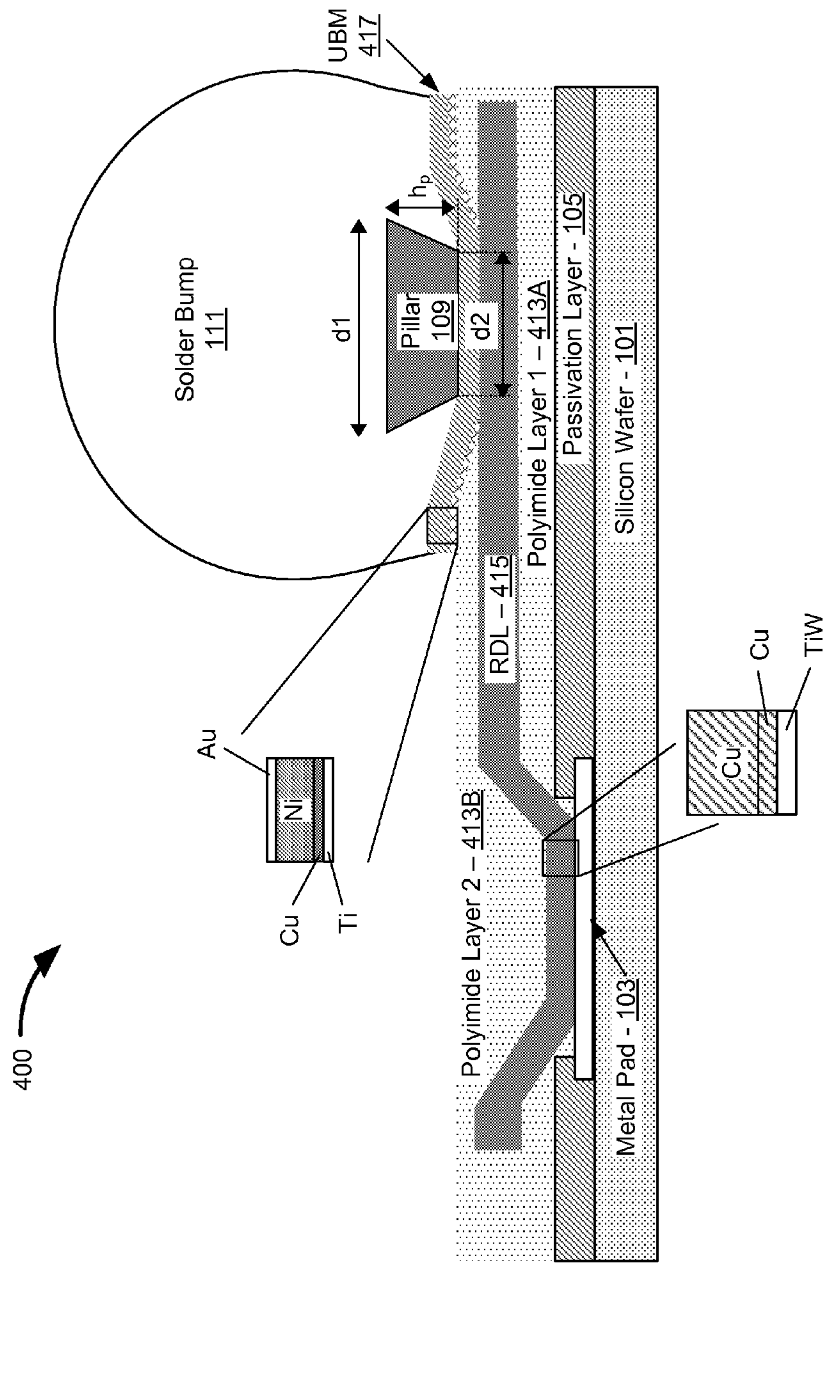

300
Solder Bump 111
d1
Pillar - 109
d2
h_p
Post - 307
d3
Solder Brace - 113
Seed Layer - 115
Passivation Layer - 105
Metal Pad - 103
Silicon Wafer - 101

FIG. 3



UBM
417
Solder Bump
111
d1
Pillar
109
d2
h_p
Polyimide Layer 1 – 413A
Passivation Layer - 105
Silicon Wafer - 101
RDL – 415
Polyimide Layer 2 – 413B
Metal Pad - 103
Au
Ni
Cu
Ti
Cu
Cu
TiW
400

FIG. 4

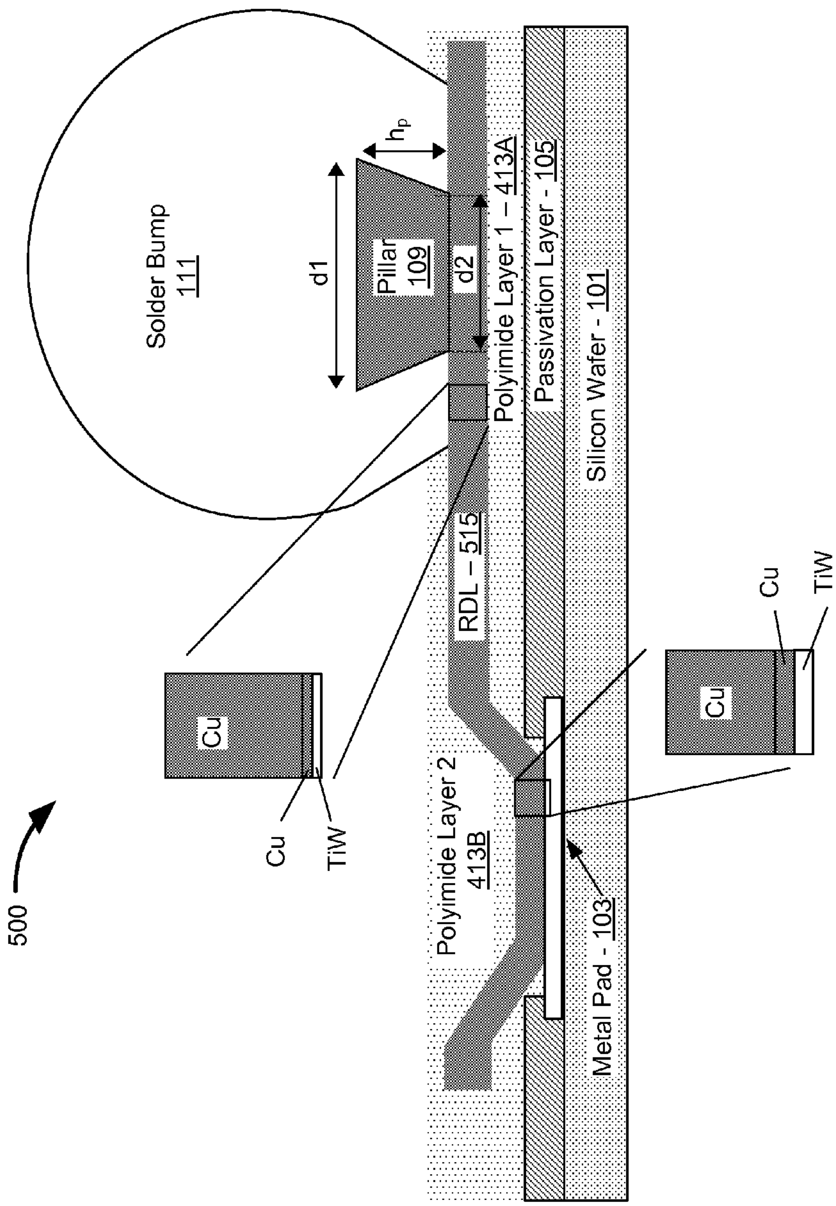

500
Solder Bump
111
Pillar
109
d1
d2
hp
Polyimide Layer 1 – 413A
Passivation Layer - 105
Silicon Wafer - 101
RDL – 515
Cu
TiW
Cu
Cu
TiW
Cu
Polyimide Layer 2
413B
Metal Pad - 103

FIG. 5

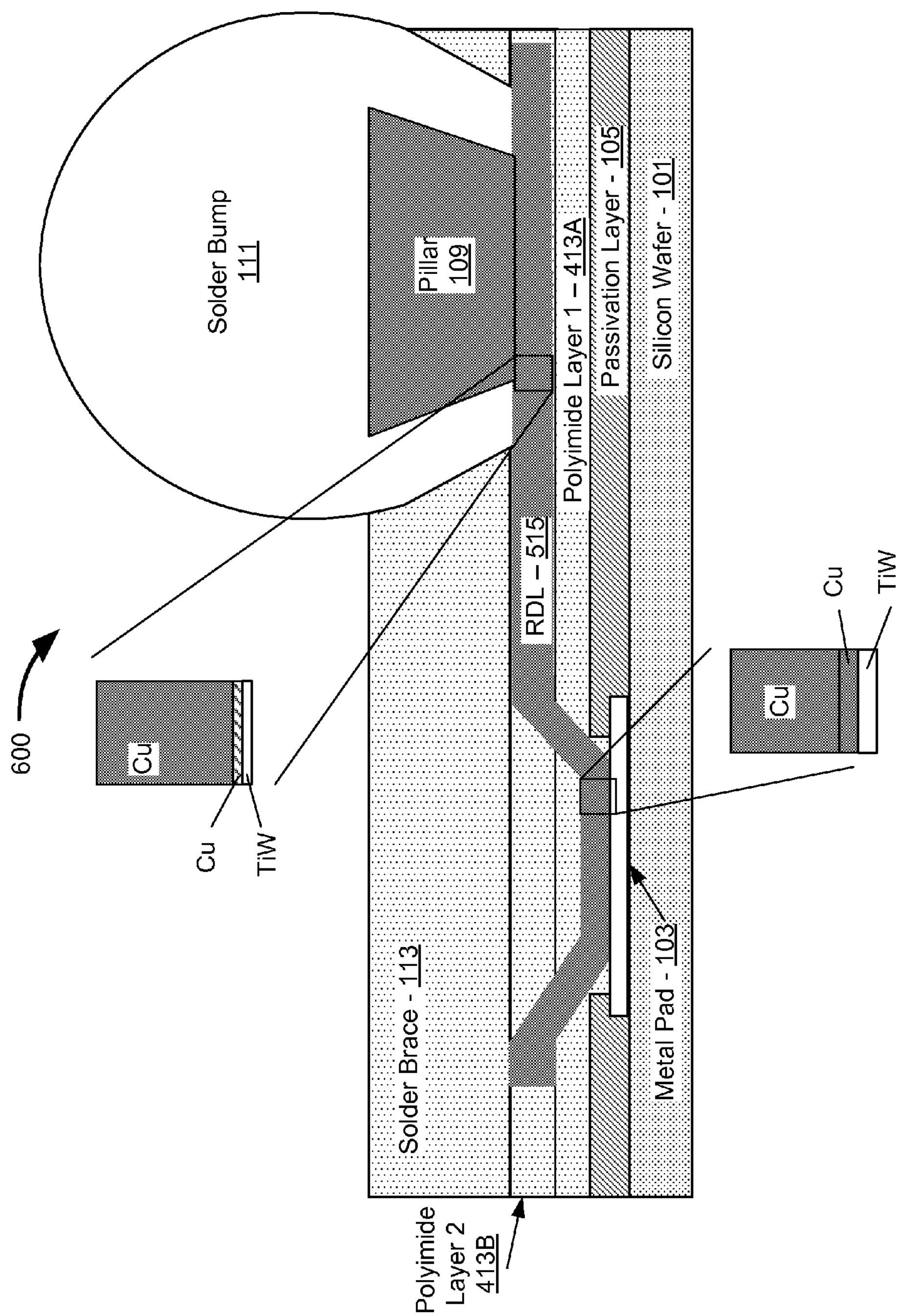

600
Solder Bump
111
Pillar
109
Polyimide Layer 1 – 413A
Passivation Layer - 105
Silicon Wafer - 101
RDL – 515
Cu
Cu
TiW
Cu
Cu
TiW
Metal Pad - 103
Solder Brace - 113
Polyimide
Layer 2
413B

FIG. 6

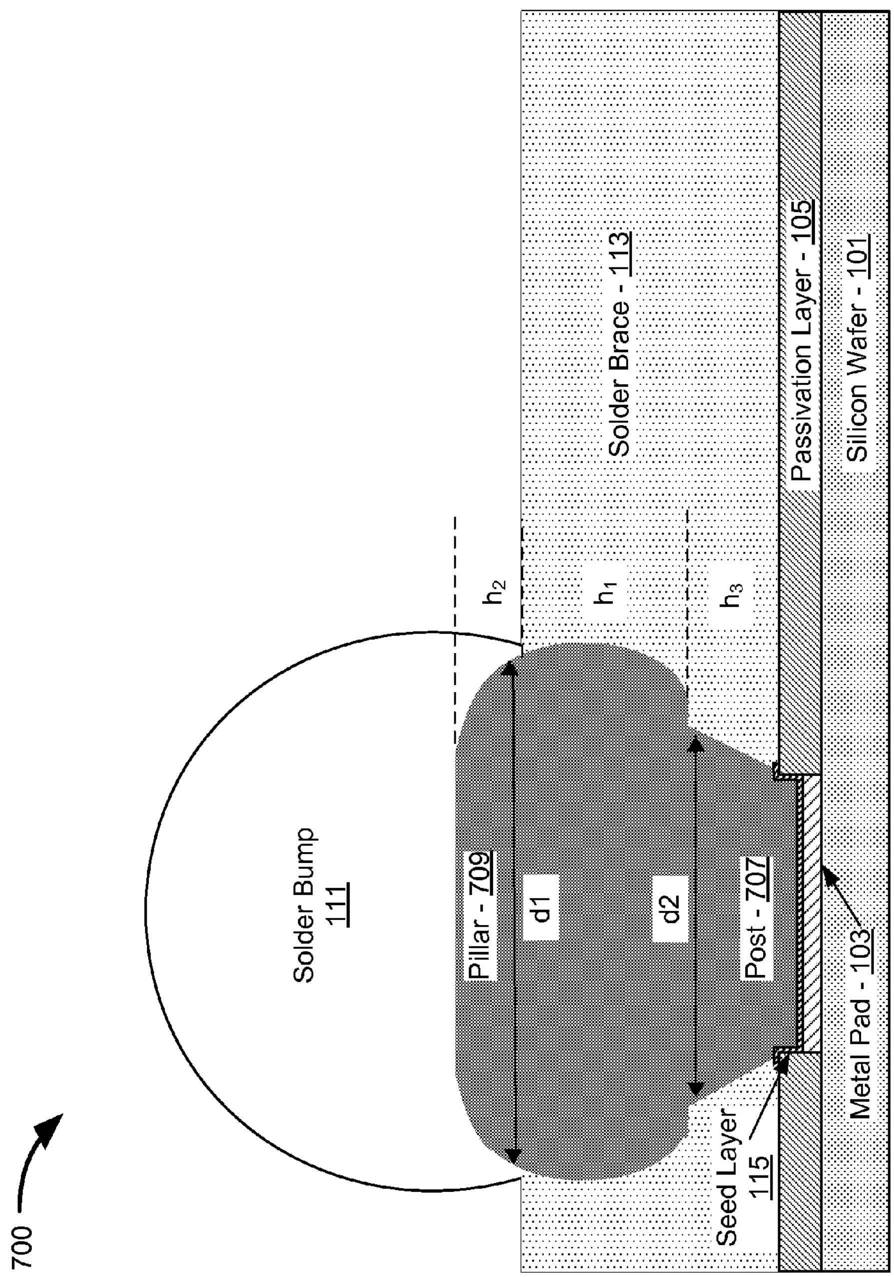

700
Solder Bump
111
Pillar - 709
d1
d2
Post - 707
h2
h1
h3
Solder Brace - 113
Passivation Layer - 105
Silicon Wafer - 101
Seed Layer
115
Metal Pad - 103

FIG. 7

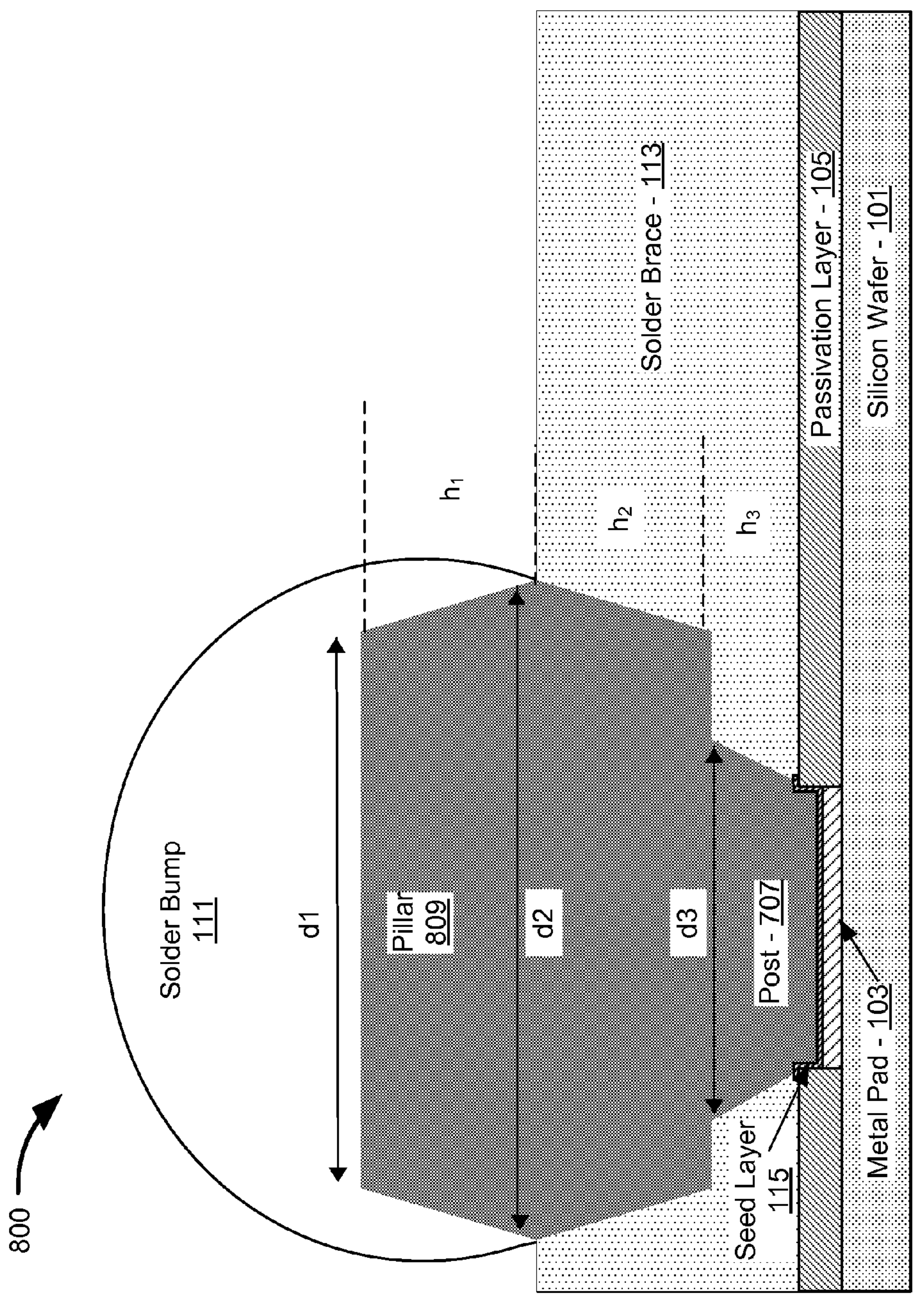

800
Solder Bump
111
Pillar
809
d1
d2
d3
Post - 707
h1
h2
h3
Solder Brace - 113
Passivation Layer - 105
Silicon Wafer - 101
Metal Pad - 103
Seed Layer
115

FIG. 8

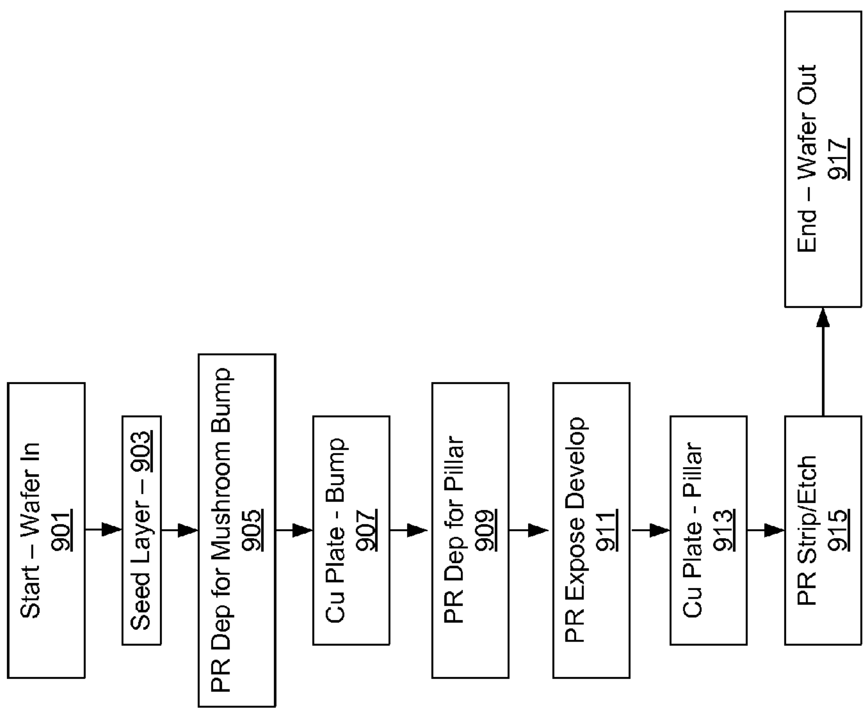
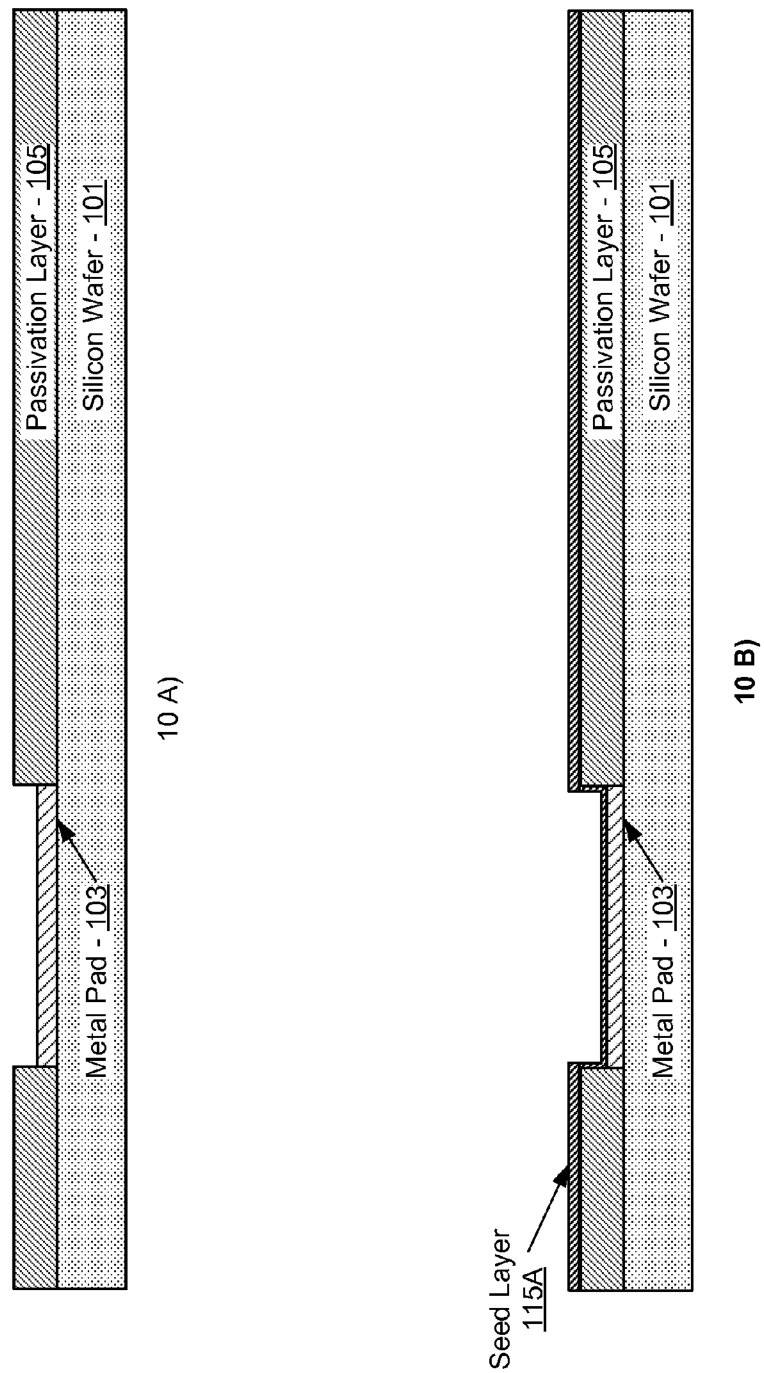

Start – Wafer In
901
Seed Layer – 903
PR Dep for Mushroom Bump
905
Cu Plate - Bump
907
PR Dep for Pillar
909
PR Expose Develop
911
Cu Plate - Pillar
913
PR Strip/Etch
915
End – Wafer Out
917

FIG. 9



Passivation Layer - 105
Silicon Wafer - 101
Metal Pad - 103
10 A)
Passivation Layer - 105
Silicon Wafer - 101
Metal Pad - 103
Seed Layer
115A
10 B)

FIG. 10A-10B

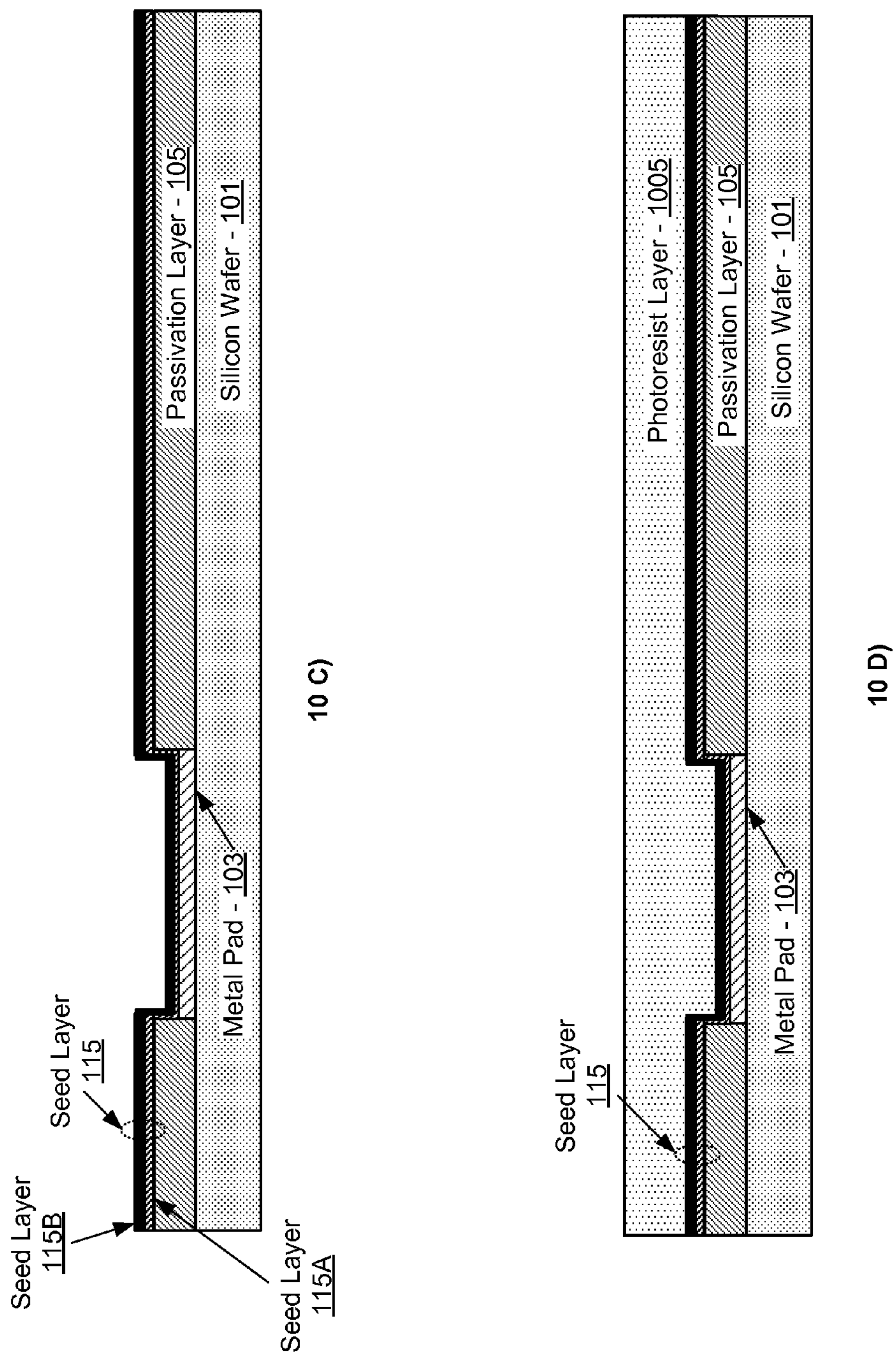

Passivation Layer - 105
Silicon Wafer - 101
Metal Pad - 103
Seed Layer 115
Seed Layer 115B
Seed Layer 115A
10 C)
Photoresist Layer - 1005
Passivation Layer - 105
Silicon Wafer - 101
Metal Pad - 103
Seed Layer 115
10 D)

FIG. 10C-10D

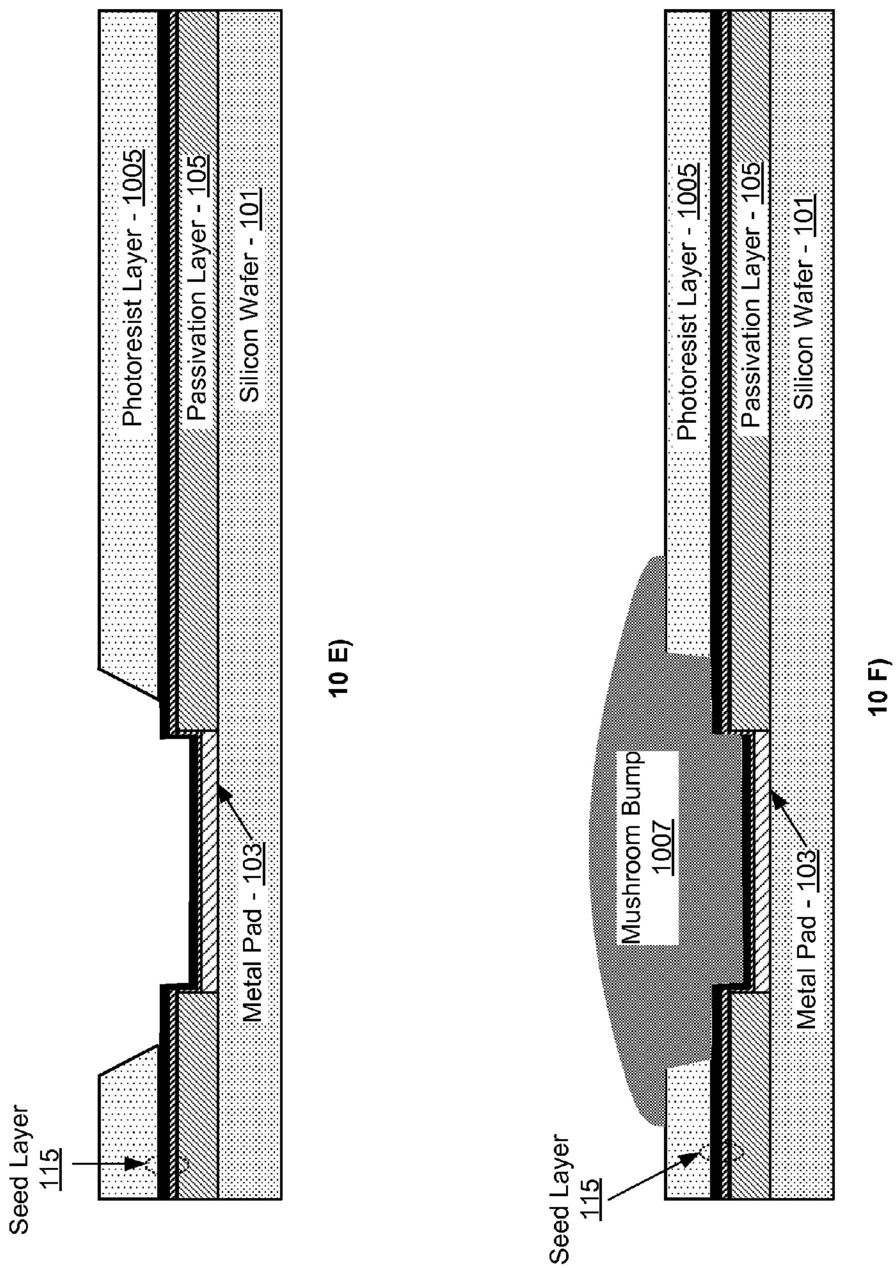
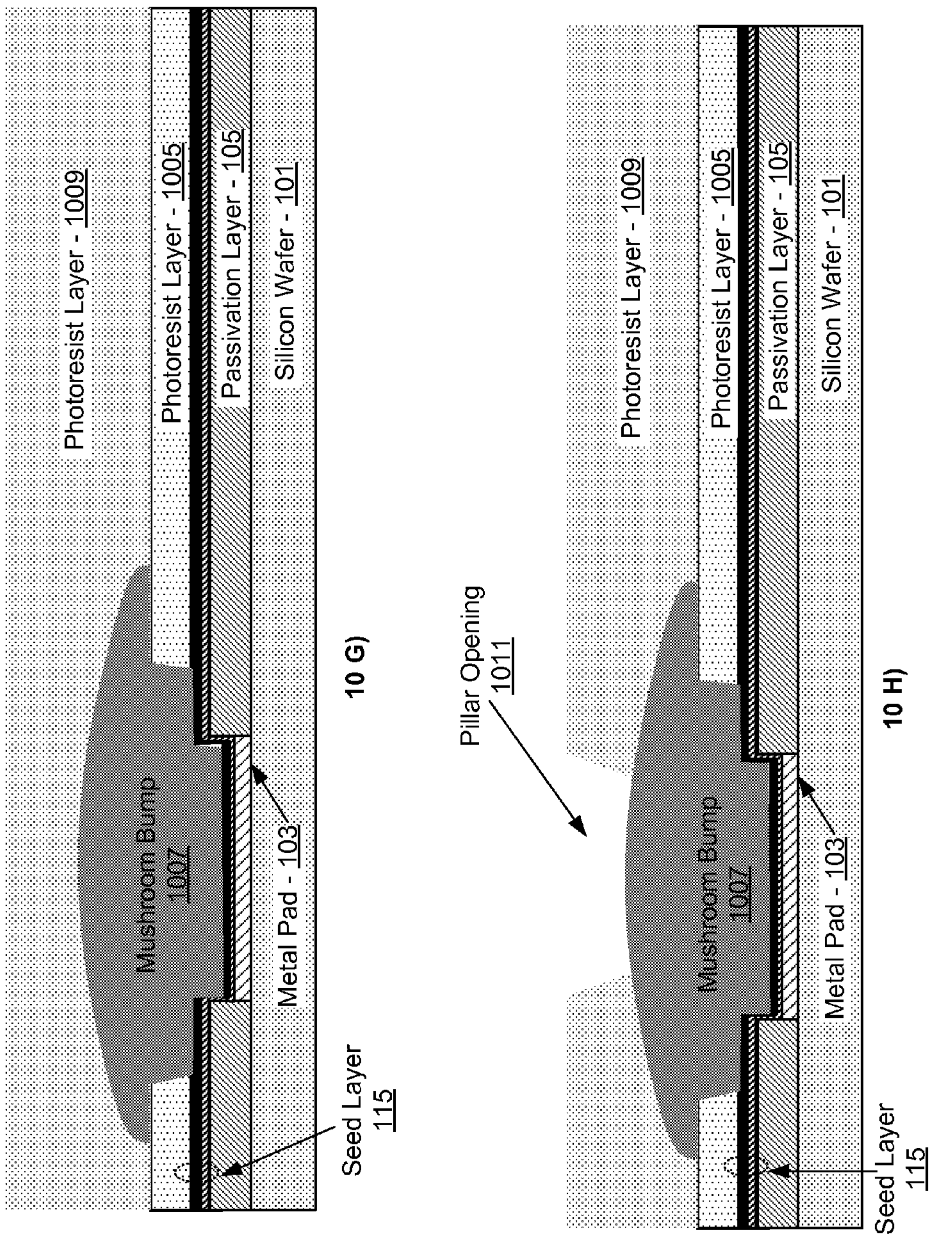
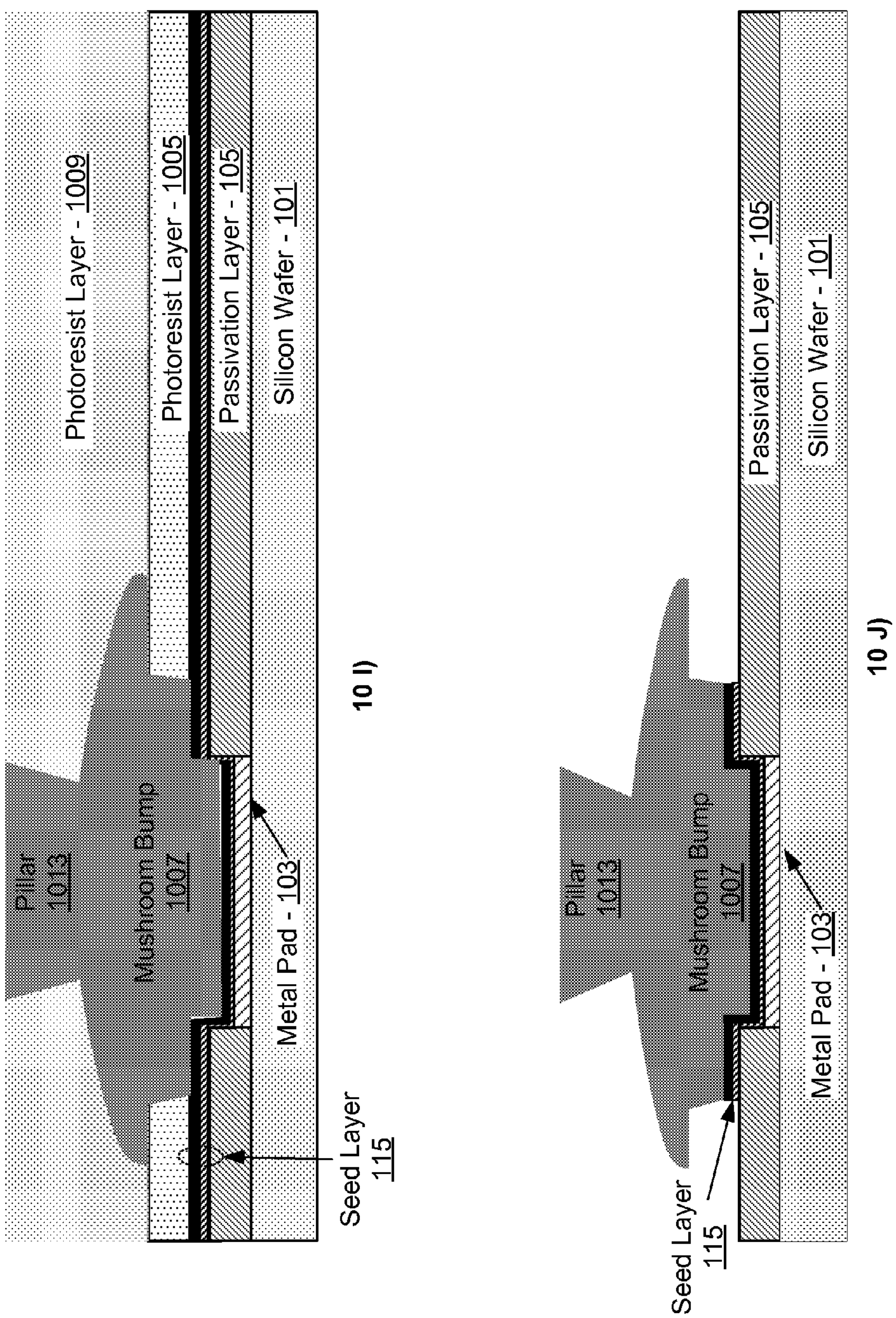

Photoresist Layer - 1005
Passivation Layer - 105
Silicon Wafer - 101
Metal Pad - 103
Seed Layer 115
10 E)
Photoresist Layer - 1005
Passivation Layer - 105
Silicon Wafer - 101
Mushroom Bump 1007
Metal Pad - 103
Seed Layer 115
10 F)

FIG. 10E-10F



Photoresist Layer - 1009
Photoresist Layer - 1005
Passivation Layer - 105
Silicon Wafer - 101
Mushroom Bump 1007
Metal Pad - 103
Seed Layer 115
10 G)
Pillar Opening 1011
Photoresist Layer - 1009
Photoresist Layer - 1005
Passivation Layer - 105
Silicon Wafer - 101
Mushroom Bump 1007
Metal Pad - 103
Seed Layer 115
10 H)

FIG. 10G-10H



Photoresist Layer - 1009
Photoresist Layer - 1005
Passivation Layer - 105
Silicon Wafer - 101
Pillar
1013
Mushroom Bump
1007
Metal Pad - 103
Seed Layer
115
10 I)
Pillar
1013
Mushroom Bump
1007
Passivation Layer - 105
Silicon Wafer - 101
Metal Pad - 103
Seed Layer
115
10 J)

FIG. 10I-10J

ROBUST PILLAR STRUCTURE FOR SEMICONDCUTOR DEVICE CONTACTS

FIELD OF THE INVENTION

Certain embodiments of the invention relate to semiconductor devices. More specifically, certain embodiments of the invention relate to methods and systems for a robust pillar structure for semiconductor device contacts.

BACKGROUND OF THE INVENTION

Semiconductor device contacts provide electrical connections between structures such as an integrated circuit die and a packaging substrate. Contacts can also provide a thermal conductance path to efficiently remove heat generated in a chip. Thermal stresses from heat generated in semiconductor die can damage these contacts.

Further limitations and disadvantages of conventional and traditional approaches will become apparent to one of skill in the art, through comparison of such systems with the present invention as set forth in the remainder of the present application with reference to the drawings.

BRIEF DESCRIPTION OF SEVERAL VIEWS OF THE DRAWINGS

FIG. **1** is a drawing illustrating a pillar on a stepped mushroom shaped post with solder brace, in accordance with an example embodiment of the invention.

FIG. **2** is a drawing illustrating a pillar on a tapered mushroom shaped post with solder brace, in accordance with an example embodiment of the invention.

FIG. **3** is a drawing illustrating a pillar on a cylindrical post with solder brace, in accordance with an example embodiment of the invention.

FIG. **4** is a drawing illustrating a pillar used in a redistribution layer contact with under bump metal, in accordance with an example embodiment of the invention.

FIG. **5** is a drawing illustrating a pillar used in a redistribution layer contact, in accordance with an example embodiment of the invention.

FIG. **6** is a drawing illustrating a pillar used in a redistribution layer contact with solder brace, in accordance with an example embodiment of the invention.

FIG. **7** is a drawing illustrating a thick mushroom shaped pillar with solder brace, in accordance with an example embodiment of the invention.

FIG. **8** is a drawing illustrating a sloped mushroom shaped pillar with solder brace, in accordance with an example embodiment of the invention.

FIG. **9** is a flow diagram illustrating example steps in fabricating a pillar structure in a metal interconnect, in accordance with an embodiment of the invention.

FIGS. **10A-10J** illustrate the pillar structure process steps of FIG. **9**.

DETAILED DESCRIPTION OF THE INVENTION

Certain aspects of the invention may be found in methods and systems for a robust pillar structure for semiconductor device contacts. Example aspects of a method in accordance with an embodiment of the invention may comprise processing a semiconductor wafer comprising one or more metal pads, wherein the processing may comprise: forming a second metal contact on the one or more metal pads;

forming a pillar on the second metal contact, and forming a solder bump on the second metal contact and the pillar, wherein the pillar extends into the solder bump. The second metal contact may comprise a stepped mushroom shaped bump, a sloped mushroom shaped bump, a cylindrical post, and/or a redistribution layer. The semiconductor wafer may comprise silicon. A solder brace layer may be formed around the second metal contact. The second metal contact may be tapered down to a smaller area at the one or more metal pads on the semiconductor wafer. A seed layer may be formed between the second metal contact and the one or more metal pads on the semiconductor wafer. The pillar may comprise copper.

FIG. **1** is a drawing illustrating a pillar on a stepped mushroom shaped post with solder brace, in accordance with an example embodiment of the invention. Referring to FIG. **1**, there is shown a metal interconnect **100** comprising a pillar **109** on a second metal contact comprising a stepped mushroom shaped bump **107** electrically connected to the metal pad **103**. The mushroom shaped bump **107** may comprise a thick layer of copper fabricated in multiple steps to result in the tapered step shape shown in FIG. **1**. There is also shown a solder bump **111** formed above and around the sides of the pillar **109**. Pillar **109** may comprise a copper pillar structure formed on the top surface of the mushroom shaped bump **107** for alleviating thermal stress in the metal interconnect **100** by introducing a "zig-zag" shaped interface between the copper of the mushroom shaped bump **107**/pillar **109** and the solder bump **111**.

The integration of the pillar **109** on the mushroom shaped bump **107** and in the solder bump **111** may result in increased solder joint reliability (SJR) The pillar **109** may, for example, have a tapered sidewall with an upper width larger than a lower width. Alternatively, for example, the pillar may have other types of tapered sidewalls and/or vertical sidewalls. The use of pillar **109** may result in better SJR for wafer-level packaging technologies as the robust pillar-like structure helps to delay failure/crack propagation during field use resulting in enhanced joint reliability. Also, due to the increased Cu thickness, this may improve electromigration performance of the joints.

The ratio of the width of the pillar **109**, indicated by d**1**, to the width of the solder bump **111**, indicated by d**2**, may be varied to optimize the improvement in the SJR. Similarly, the height of the pillar **109**, indicated as h_p, may also be varied in optimizing SJR. In an example scenario, the width of pillar **109**, d**1**, may equal the width of the metal pad **103**, shown as d**3**. In an example embodiment, the height of the steps of the mushroom shaped bump may be 10 microns, and the height of pillar **109** may be 20-30 microns.

A passivation layer **105** and a solder brace layer **113** may surround the mushroom shaped bump **107**. The passivation layer **105** may comprise an insulating dielectric material on the surface of the silicon wafer **101**. The passivation layer **105** may provide electrical and mechanical isolation for the various devices and conductive layers at the surface of the silicon wafer **101**, while openings in the passivation layer **105** allow for metal pads such as the metal pad **103** and seed layer **115** to provide electrical connection between circuitry in the wafer **101** and external devices or circuitry via the mushroom shaped bump **107**, pillar **109**, and the solder bump **111**.

The solder brace layer **113** may fill in underneath the stepped sidewall of the mushroom shaped bump **107** and may comprise an insulating dielectric material that may be more rigid than polyimide materials. Solder brace may refer to a unique type of repassivation that may eliminate the need for underfill and may be used to improve the reliability of the solder joints between the chip (integrated circuit and package) and the circuit board. Solder brace materials may have several unique properties that make them different from other repassivation materials.

It should be understood that the shape of the mushroom shaped bump **107** with pillar **109** shown in FIG. **1** is just one example of the use of a pillar for improved SJR, and the types of contacts contemplated by this disclosure are not limited to the mushroom shaped bump in FIG. **1**. An example detailed process flow for such a structure is illustrated in FIG. **10**.

The silicon wafer **101** may comprise a customer-supplied wafer, for example, with a plurality of integrated circuit die, where the metal pad **103** provides an electrical contact to the circuitry in the silicon wafer **101**. The silicon wafer **101** may be processed using a wafer-level chip-scale process (WLCSP), which may involve depositing metal contact layers and/or bumps, for example consisting of copper layer structures that are thick enough for receiving a solder ball **110** and withstanding a reflow process without being depleted in the process. The silicon wafer **101** may then be subjected to a thermal cycle during which time the solder bump **111** melts and then cools in a well-defined shape on top of the pillar **109** and the mushroom shaped bump **107**. The seed layer **115** may also be referred to herein as an under bump metal (UBM).

FIG. **1** also shows a seed layer **115** that may be applied on top of the metal pad **103**. The seed layer **115** may be the first layer added in the wafer-level chip scale packaging process. The seed layer **115** may include an adhesion layer, for example, comprised of titanium (Ti) or Ti-Tungsten (TiW), which may serve to adhere the mushroom shaped bump **107** firmly to the silicon wafer **101** while still being electrically conductive. The seed layer **115** may also include another conductive layer, for example, comprised of a metal such as copper.

The final integrated circuit and package may be mounted on a circuit board using heat to melt the solder bumps, such as the solder bump **111**, and attach the integrated circuit and package (collectively, the "chip") to the circuit board. An underfill material may be inserted between the chip and the circuit board, for example to deal with the differences in thermal expansion coefficients between the chip and the circuit board that may lead to undesirable pressure on one or more bumps of the chip package. The underfill material may act like glue, holding the chip firmly to the circuit board, absorbing some pressure and resisting expansion of the board in the area of the chip. Portions of the present disclosure describe one or more systems, methods, routines and/or techniques for forming a pillar on a mushroom shaped bump. In some embodiments, the vertical thickness, h_p, and the width at the top and bottom of the pillar, may be important, for example, to optimize SJR (Solder Joint Reliability). In addition, pillar **109** may improve electromigration issues due to the increased copper thickness and the reduced width of the opening in the passivation layer **105** in conjunction with the mushroom shaped bump **107** and solder brace **113** may further improve SJR.

FIG. **2** is a drawing illustrating a pillar on a tapered mushroom shaped post with solder brace, in accordance with an example embodiment of the invention. Referring to FIG. **2**, there is shown a metal interconnect **200** comprising the solder bump **111**, pillar **109**, a mushroom shaped bump **207**, the seed layer **115** and the metal pad **103**. There is also shown the silicon wafer **101**, the passivation layer **105**, and the solder brace layer **113**. Like-numbered elements of FIG. **2** are substantially similar to those shown in FIG. **1**, and the mushroom shaped bump **207** may be substantially similar to the mushroom shaped bump shown in FIG. **1**, but with a tapered sidewall as opposed to a stepped sidewall.

As with the stepped sidewall mushroom shaped bump structure of FIG. **1**, the ratio of the width of pillar **109**, d**1**, to the width of the solder bump **111**, d**2**, may be varied to optimize the improvement in the SJR. Similarly, the height of pillar **109**, h_p, may also be varied in optimizing SJR. In an example scenario, the width of pillar **109**, d**1**, may equal the width of the metal pad **103**, d**3**. In another example scenario, the height of the "lip", h**1**, of the mushroom shaped bump **207** may be 10 microns and the height of the tapered "stem," h**2**, of the mushroom shaped bump **207** may be 20 microns, while the height, h_p, of pillar **109** may be 20-30 microns.

The "necking" or tapering of the mushroom shaped bump **207** may improve SJR due to the reduced via size in the passivation layer **105** and increased solder bump layer opening above the mushroom shaped bump **207**.

FIG. **3** is a drawing illustrating a pillar on a cylindrical post with solder brace, in accordance with an example embodiment of the invention. Referring to FIG. **3**, there is shown a metal interconnect **300** comprising the solder bump **111**, the pillar **109**, a second metal contact comprising a cylindrical post **307**, and the metal pad **103**. There is also shown the silicon wafer **101**, the passivation layer **105**, and the solder brace layer **113**. Like-numbered elements of FIG. **3** are substantially similar to those shown in FIGS. **1** and **2**. The cylindrical post **307** may comprise a cylindrical copper post with a tapered sidewall as opposed to the mushroom shaped bumps of FIGS. **1** and **2**.

As with the stepped sidewall mushroom shaped bump structure of FIG. **1** or the tapered mushroom shaped bump **209** of FIG. **2**, the ratio of the width of pillar **109**, d**1**, to the width of the solder bump **111**, d**2**, may be varied to optimize the improvement in the SJR. Similarly, the height of pillar **109**, h_p, may also be varied in optimizing SJR. In an example scenario, the width of pillar **109**, d**1**, may equal the width of the metal pad **103**, d**3**. In another example scenario, the height of the cylindrical post **307** may be 30 microns, while the height, h_p, of pillar **109** may be 20-30 microns.

FIG. **4** is a drawing illustrating a pillar used in a redistribution layer contact with under bump metal, in accordance with an example embodiment of the invention. Referring to FIG. **4**, there is shown a metal interconnect **400** comprising the solder bump **111**, pillar **109**, an under bump metal (UBM) **417**, and a second metal contact comprising a redistribution layer (RDL) **415**. There is also shown the silicon wafer **101**, the metal pad **103**, the passivation layer **105**, and polyimide layers **413**A and **413**B. The insets show example metal stacks for the RDL **415** comprising a copper/titanium/tungsten stack and the UBM **417** comprising a gold layer on plated nickel with a copper/titanium seed layer.

The RDL **415** may comprise a copper conductive path that provides electrical connectivity between the solder bump **111** and the metal pad **103** and may extend to multiple levels in the metal/dielectric layers on the silicon wafer **101**. In this manner, the solder bumps may be placed in locations away from metal pads on the wafer so that a high-density array of solder balls may be utilized independent of the location of the metal pads.

The polyimide layers **413**A and **413**B may comprise dielectric layers for providing insulation between various RDL traces and layers. In another example scenario, the polyimide layers may instead comprise another polymer such as polybenzoxale (PBO).

The UBM **417** may comprise a metal layer stack for providing a good mechanical and electrical connection between the solder bump **111** and the RDL **415**. The concave shape of the UBM **417** due to the polyimide layer **2 413**B may assist in creating the round solder bump shape following a reflow process.

As with the mushroom shaped bump embodiments shown in FIGS. **1-3**, pillar **109** may improve solder joint reliability by providing a "zig-zag" interface between the solder bump **111** and the UBM **417**. The height, h_p, of the pillar **109** and the ratio of the width, d**1**, at the top of pillar **109** to the width, d**2**, at the bottom may be varied to optimize SJR. Lateral strain caused by different coefficients of thermal expansion of the silicon wafer **101** and a package or substrate it is bonded to may cause physical failure of conventional contacts. By incorporating the pillar **109** in the solder bump **111**, the strain fields may be spread over a larger area with same contact width, and may reduce current crowding.

FIG. **5** is a drawing illustrating a pillar used in a redistribution layer contact, in accordance with an example embodiment of the invention. Referring to FIG. **5**, there is shown a metal interconnect **500** comprising the solder bump **111**, the pillar **109**, and the second metal contact comprising the RDL **515**. There is also shown the silicon wafer **101**, the metal pad **103**, the passivation layer **105**, and the polyimide layers **413**A and **413**B. The insets show example metal stacks for the RDL **515** comprising a copper/titanium/tungsten stack.

In this example scenario, pillar **109** and the solder bump **111** may be placed directly on the RDL **515** without an under bump metal, where the copper in the RDL **515**, as shown in the inset, may be significantly thicker than in the RDL **415** shown in FIG. **4**. In an example scenario, the copper in the RDL **515** may be on the order of 9 microns thick as compared to 3 microns in the RDL **415**.

As with the embodiments shown in FIGS. **1-4**, pillar **109** may improve solder joint reliability by providing a "zig-zag" interface between the solder bump **111** and the RDL **515**. The height, h_p, of the pillar **109** and the ratio of the width, d**1**, at the top of pillar **109** to the width, d**2**, at the bottom may be varied to optimize SJR. Lateral strain caused by different coefficients of thermal expansion of the silicon wafer **101** and a package or substrate it is bonded to may cause physical failure of conventional contacts. By incorporating the pillar **109** in the solder bump **111**, the strain fields may be spread over a larger area with the same contact width, and may reduce current crowding.

FIG. **6** is a drawing illustrating a pillar used in a redistribution layer contact with solder brace, in accordance with an example embodiment of the invention. Referring to FIG. **6**, there is shown a metal interconnect **600** comprising the solder bump **111**, the pillar **109**, and the second metal contact comprising the RDL **515**. There is also shown the silicon wafer **101**, the metal pad **103**, the passivation layer **105**, the solder brace layer **113**, and the polyimide layers **413**A and **413**B. The insets show example metal stacks for the RDL **515** comprising a copper/titanium/tungsten stack.

In this example scenario, pillar **109** and the solder bump **111** may be placed directly on the RDL **515** without an under bump metal, where the copper in the RDL **515**, as shown in the inset, may be significantly thicker than in the RDL **415** shown in FIG. **4**. In an example scenario, the copper in the RDL **515** may be on the order of 9 microns thick as compared to 3 microns in the RDL **415**. Furthermore, the solder brace layer **113** may surround the solder bump **111**.

As with the embodiments shown in FIGS. **1-5**, pillar **109** may improve solder joint reliability by providing a "zig-zag" interface between the solder bump **111** and the RDL **515**. The height, h_p, of the pillar **109** and the ratio of the width, d**1**, at the top of pillar **109** to the width, d**2**, at the bottom may be varied to optimize SJR. Lateral strain caused by different coefficients of thermal expansion of the silicon wafer **101** and a package or substrate it is bonded to may cause physical failure of conventional contacts. By incorporating the pillar **109** in the solder bump **111**, the strain fields may be spread over a larger area with same contact width, and may reduce current crowding.

Additionally, the solder brace layer **113** may surround the solder bump **111** and provide a more rigid structure around the bumps. In an example scenario, the polyimide layers **413**A and **413**B may be on the order of 5 microns thick and the solder brace layer **113** may be 20-30 microns thick. Solder brace material is much less prone to cracking than is customer passivation or silicon, nitride or the like. In other words, solder brace material is adapted to more effectively absorb stress and strain than is customer passivation or silicon, nitride or the like, which may increase solder joint reliability (SJR).

FIG. **7** is a drawing illustrating a thick mushroom shaped pillar with solder brace, in accordance with an example embodiment of the invention. Referring to FIG. **7**, there is shown a metal interconnect **700** comprising the solder bump **111**, mushroom shaped pillar comprising the pillar **709**, a second metal contact comprising a cylindrical post **707**, and the metal pad **103**. There is also shown the silicon wafer **101**, the passivation layer **105**, the solder brace layer **113**, and the seed layer **115**. Like-numbered elements of FIG. **7** are substantially similar to those shown in FIGS. **1-6**. The cylindrical post **707** may comprise a cylindrical copper post with a tapered sidewall that is formed on the seed layer **115** and supports the mushroom shaped pillar **709**.

As with the pillars described in FIGS. **1-6**, the shape of the mushroom shaped pillar **709**, d**1**, to the width of the solder bump **111**, d**2**, may be varied to optimize the improvement in the SJR. Similarly, the height of pillar **709**, h_p, that extends into the solder bump **111** may also be varied in optimizing SJR.

FIG. **8** is a drawing illustrating a sloped mushroom shaped pillar with solder brace, in accordance with an example embodiment of the invention. Referring to FIG. **8**, there is shown a metal interconnect **800** comprising the solder bump **111**, a sloped mushroom shaped pillar comprising the pillar **809**, the second metal contact comprising the cylindrical post **707**, and the metal pad **103**. There is also shown the silicon wafer **101**, the passivation layer **105**, the solder brace layer **113**, and the seed layer **115**. Like-numbered elements of FIG. **8** are substantially similar to those shown in FIGS. **1-7**. The cylindrical post **707** may comprise a cylindrical copper post with a tapered sidewall that is formed on the seed layer **115** and supports the sloped mushroom shaped pillar **809**.

Different embodiments, for example the embodiments of FIGS. **2-8**, may achieve different levels of improved SJR, with pillar dimensions, mushroom bump/post complexity, and solder bump dimensions may be varied to determine a preferred SJR when cost and process complexity tradeoffs are considered.

As with the pillars described in FIGS. **1-7**, the shape and dimensions of the sloped mushroom shaped pillar **809** may be varied to optimize SJR, where the strain from thermal expansion and contraction may be diffused over a larger interface between the solder bump **111** and the sloped mushroom shaped pillar **809**. For example, the height of the sloped mushroom shaped pillar **109**, h_p, that extends into the solder bump **111** may be varied in optimizing SJR. Similarly, the width of the pillar d**1**, at the top of the pillar compared to the width of the pillar, d**2**, at the base of the solder bump **111**, may also be varied to optimize the improvement in the SJR. In addition, the utilization of the solder brace layer **113** may enable a narrow opening in the passivation layer **105** while still allowing a larger width, d**3**, of the top of the cylindrical post **707**.

FIG. **9** is a flow diagram illustrating example steps in fabricating a pillar structure in a metal interconnect, in accordance with an embodiment of the invention. FIGS. **10**A-**10**J illustrate the pillar structure process steps of FIG. **9**. Referring to FIG. **9**, the process begins with start step **901**, where a silicon wafer may be input into the process with a passivation layer comprising openings for metal contacts to be formed within, as shown in FIG. **10** A). In step **903**, a seed layer **915**, comprising seed layers **115**A and **115**B, may be deposited on the wafer on top of the passivation layer **105** as well as the openings, as shown in FIGS. **10** B) and **10** C). In an example scenario, the seed layer may comprise a copper (seed layer **115**A) and titanium/tungsten (seed layer **115**B) stack, as shown in FIGS. **10** C) to **10** I).

In step **905**, a photoresist layer **1005** may be spun on the deposited seed layer **115** to generate a mask layer for defining a bump structure, as shown in FIG. **10** D), such as a mushroom shaped bump. The photoresist layer **1005** may be exposed to a UV light source through a mask such that exposed photoresist will be removed in a subsequent develop process, in a positive photoresist example. Following development, the wafer may be baked to harden the remaining photoresist, resulting in the structure shown in FIG. **10** E).

In step **907**, copper may be plated/deposited on the PR masked structure, thereby filling in the regions not covered by photoresist, resulting in a mushroom or "nail head" shape within the opening and extending beyond the opening on top of the photoresist layer **1005**, as shown in FIG. **10**F.

In step **909**, a second photoresist layer may be deposited, as shown by photoresist layer **1009** in FIG. **10** G), for defining a pillar structure to extend into a subsequent solder bump. Step **911** comprises a PR expose and develop step, where portions of the photoresist layer may be exposed to an ultraviolet light source through a mask for removal of exposed portions, such as the pillar opening **1011**, during a subsequent develop process. Following development, the wafer may be baked to harden the remaining photoresist, resulting in the structure shown in FIG. **10** H).

In step **913** a plating or deposition process may be utilized to fill the pillar opening **1011** with copper, thereby forming a pillar on the mushroom bump **1007**, with the resulting pillar **1013** shown in FIGS. **10** I) and **10** J).

In step **915**, the photoresist layers **1005** and **1009** may be removed in a photoresist strip process, followed by a metal etch process that may remove the exposed portions of the seed layer **115**, such that the only portion of the seed layer **115** remaining is under the mushroom bump **1007**. Step **915** is followed by end step **917** where the completed wafer shown in FIG. **10** I) is the output.

In an embodiment of the invention, methods are disclosed for a robust pillar structure for semiconductor device contacts and may comprise processing a semiconductor wafer comprising one or more metal pads, wherein the processing may comprise: forming a second metal contact on the one or more metal pads; forming a pillar on the second metal contact, and forming a solder bump on the second metal contact and the pillar, wherein the pillar extends into the solder bump. The second metal contact may comprise a stepped mushroom shaped bump, a sloped mushroom shaped bump, a cylindrical post, and/or a redistribution layer. The semiconductor wafer may comprise silicon. A solder brace layer may be formed around the second metal contact. The second metal contact may be tapered down to a smaller area at the one or more metal pads on the semiconductor wafer. A seed layer may be formed between the second metal contact and the one or more metal pads on the semiconductor wafer. The pillar may comprise copper.

While the invention has been described with reference to certain embodiments, it will be understood by those skilled in the art that various changes may be made and equivalents may be substituted without departing from the scope of the present invention. In addition, many modifications may be made to adapt a particular situation or material to the teachings of the present invention without departing from its scope. Therefore, it is intended that the present invention not be limited to the particular embodiments disclosed, but that the present invention will include all embodiments falling within the scope of the appended claims.

What is claimed is:

1. A method for forming a semiconductor contact, the method comprising:
- processing a semiconductor wafer comprising a metal pad, wherein said processing comprises:
  - forming a metal contact on the metal pad;
  - forming a pillar on the metal contact, wherein the pillar is tapered down such that its width decreases toward the metal contact and wherein the metal contact comprises a sloped mushroom shaped bump or a stepped mushroom shaped bump; and
  - forming a solder bump on the metal contact and the pillar, wherein the pillar extends into the solder bump.

2. The method according to claim **1**, wherein the metal contact comprises the stepped mushroom shaped bump.

3. The method according to claim **1**, wherein the metal contact comprises the sloped mushroom shaped bump.

4. The method according to claim **1**, wherein the metal contact comprises a cylindrical post.

5. The method according to claim **1**, comprising forming a solder brace layer around the metal contact.

6. The method according to claim **1**, wherein the metal contact is tapered down to a smaller area at the metal pad.

7. The method according to claim **1**, comprising forming a seed layer between the metal contact and the metal pad.

8. The method according to claim **1**, wherein the pillar comprises copper.

9. An electronic device comprising:
- a semiconductor die comprising a metal pad;
- a metal contact formed on the metal pad; and
- a pillar formed on the metal contact, wherein the pillar extends into a solder bump also formed on the metal contact and is tapered down such that its width decreases toward the metal contact and wherein the metal contact comprises a sloped mushroom shaped bump or a stepped mushroom shaped bump.

10. The device according to claim **9**, wherein the metal contact comprises the stepped mushroom shaped bump.

11. The device according to claim **9**, wherein the metal contact comprises the sloped mushroom shaped bump.

12. The device according to claim **9**, wherein the metal contact comprises a cylindrical post.

13. The device according to claim **9**, comprising a solder brace layer around the metal contact.

14. The device according to claim **9**, wherein the metal contact is tapered down to a smaller area at the metal pad on the semiconductor die.

15. The device according to claim **9**, comprising a seed layer between the metal contact and the metal pad on the semiconductor die.

16. A device for providing electrical contact, the device comprising:

a semiconductor die comprising a metal pad;

a mushroom shaped contact formed on the metal pad; and

a copper pillar formed on the mushroom shaped contact, wherein the copper pillar extends into a solder bump also formed on the mushroom shaped contact and the copper pillar is wider at a top surface that is in contact with the solder bump than at a bottom surface.

17. A method for forming a semiconductor contact, the method comprising:

processing a semiconductor wafer comprising a metal pad, wherein said processing comprises:

forming a metal contact on the metal pad, wherein the metal contact comprises at least one of a stepped mushroom shaped bump or a sloped mushroom shaped bump;

forming a pillar on the metal contact, and

forming a solder bump on the metal contact and the pillar, wherein the pillar extends into the solder bump.

18. An electronic device comprising:

a semiconductor die comprising a metal pad;

a metal contact formed on the metal pad, wherein the metal contact comprises at least one of a stepped mushroom shaped bump or a sloped mushroom shaped bump; and

a pillar formed on the metal contact, wherein the pillar extends into a solder bump also formed on the metal contact.

19. The method according to claim **17**, wherein the metal contact comprises the stepped mushroom shaped bump.

20. The method according to claim **17**, wherein the metal contact comprises the sloped mushroom shaped bump.

21. The electronic device according to claim **18**, wherein the metal contact comprises the stepped mushroom shaped bump.

22. The electronic device according to claim **18**, wherein the metal contact comprises the sloped mushroom shaped bump.

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